REMARKS/ARGUMENTS

Claims 1-20 are pending in this application. The Office Action, dated May 6, 2005: rejected Claims 1, 5-8 and 12-20 under 35 USC § 102(b) and objected to Claims 2-4 and 9-11 as based on a rejected base claim but are otherwise allowable. Applicant thanks the Examiner for the review and indication of allowable subject matter for Claims 2-4 and 9-11. Applicant has amended Claims 1, 13 and 17 to further clarify the invention. The objections and rejections are believed to be overcome for the reasons stated below. No new matter is added.

Objection of Claims 2-4 and 9-11

The Office Action objected to Claims 2-4 and 9-11 as being dependent upon a rejected base claim, but noted these claims would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims. Applicant has amended base Claim 1 and believes it to be in proper form for allowance as explained bellow. Claims 2-4 and 9-11 depend from and further limit amended Claim 1 and should be allowable for at least that reason as well as any additional limitations they recite.

Rejection of Claims 1, 5-8, and 12-20 under 35 USC § 102(b)

Claims 1, 5-8 and 12-20 are rejected under 35 USC § 102(b) as being anticipated by *D'Angelo* (US Patent No. 6,166,530). Claims 1, 13 and 17 have been amended. Claims 5-8 and 12-20 depend from Claims 1, 13 and 17.

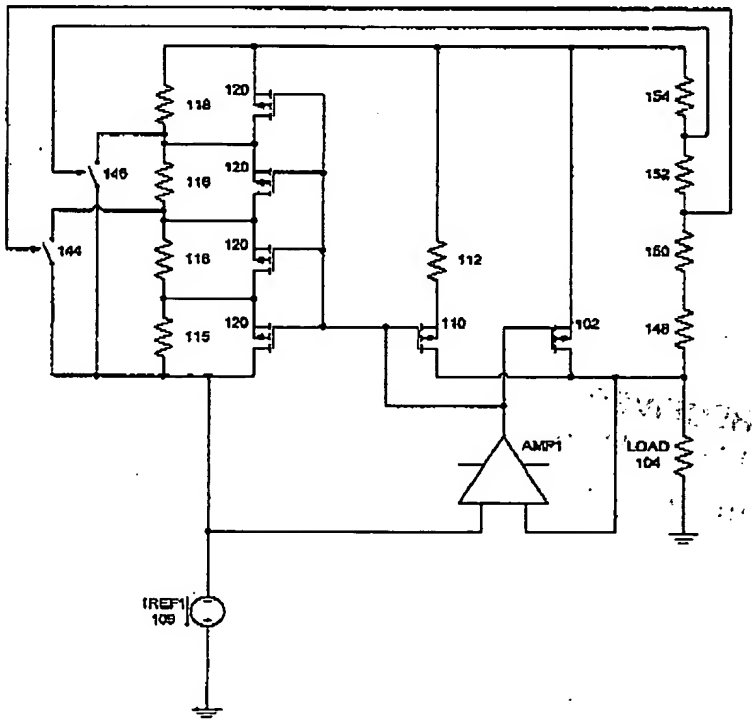
Claim 1 recites "a **differential** comparator circuit that includes: a first input that is coupled to the load circuit, a second input that is coupled to the sense signal, and an output that is

associated with the short circuit detection signal, wherein the comparator circuit is arranged to assert the **short-circuit detection signal as a logic level** when the sense signal indicates that the short-circuit condition is detected across the load circuit." A differential comparator is a circuit that compares the relative amplitude of two analog inputs, an inverting input and a non-inverting input, uniquely determining which input is larger while continuously outputting one of two logic levels. *D'Angelo* does not teach a differential comparator as is recited in amended Claim 1.

The Office Action states that *D'Angelo* teaches "a comparator (140-146)." Transistors 140-146, however, are not a differential comparator but rather are "a number of bypass switches in the form of MOSFETSs" (See *D'Angelo* at col. 6, row 25-26). The bypass switches 140-146 function in a manner wholly different than that of a comparator. Rather than differentially comparing two inputs, the switches 140-146 successively short out circuits in parallel with them as Vout falls (See *D'Angelo* at col. 6, row 42-48). For example, "When Vout reaches a threshold drop below node 128 MOSFET 140 turns on, shorting out the first parallel circuit 116" (See *D'Angelo* at col. 6, row 45-48). Successively shorting out of parallel circuits 116 has the net effect of compensating an output current for nonlinearity introduced "as the current through pilot circuit 106 increases the voltage drop across pilot resistor 112", not operating as a differential comparator (See *D'Angelo* at col. 5, rows 18-22). The operation of switches 140-146 are in **no manner similar** to that of a differential comparator as is recited in Applicant's Claim 1. Moreover, they have completely different principles of operation that are incompatible with each other.

In addition, the switches 140-146 do not have both **inverting** and **non-inverting** inputs. Rather each switch as a single input at its gate. Similarly, the switches 140-146 do not have a logic level output. Rather, each transistor provides discrete adjustment to the effective resistance in series with Iref, which shorts out a parallel circuit and changes an analog voltage Vref. In no way is this equivalent to a **logic level output**, as is recited in amended Claim 1.

A simplified diagram is provided to assist in understanding the circuits of FIG. 5 from the *D'Angelo* reference. All simplifications of this diagram are based solely on the express suggestions of *D'Angelo* and basic principles of electrical engineering and are thus fully supported by the reference. The Examiner is respectfully requested to fully consider Applicant's discussion of *D'Angelo* that follows below.



As clearly described by D'Angelo, transistors 144 and 146 operate as bypass switches, and are illustrated as such above (See *D'Angelo* at col. 6, row 25-26). As further suggested by D'Angelo, transistors 148 - 154 are arranged to operate as a voltage divider, so they may be represented as series resistors for simplicity, where the tap point in the voltage divider controls the actuation of the bypass switches, and are illustrated as resistors above (See *D'Angelo* at col. 7, row 1-4). From this figure, it can more clearly be seen that transistors 144 and 146 operate as bypass switches to successively short parallel circuits 116 and transistors 120 as described by D'Angelo (See *D'Angelo* at col. 6, row 25-48). *D'Agnelo* does not teach a differential comparator with a logic level output as described in Applicant's Claim 1.

Further, transistors 148 - 152 are not a current sense circuit as stated in the Office Action, and instead these transistors are diode connected devices that operate as a voltage divider circuit (see *D'Angelo* col. 6, lines 32-39). The voltage divider functions as a **voltage sense circuit**. Transistors 148-152 are arranged to sense voltage Vout relative to Vin, separated by a diode threshold. "Thus, the source-drain voltage across each of MOSFETs 148, 150, 152 and 154 is approximately equal to a threshold voltage drop" (See *D'Angelo* at col. 6, row 37-39). As transistors 148-152 are a voltage divider circuit that senses voltage, not current, "resistors might be used in place of MOSFETs 148, 150, 152 and 154" (See *D'Angelo* at col. 7, rows 1-4). *D'Angelo* does not teach a **current sense circuit** as described in Applicant's Claim 1.

In addition, element 110 does not meet the structural limitations of the first transistor circuit described in Applicant's Claim 1. Although element 110 is in fact a first transistor, the structural limitations of "a first transistor circuit" from Applicant's Claim 1 requires that the first

transistor circuit be arranged in relation to the remaining claim elements. Applicant's Claim 1 does not call merely for a transistor, and instead calls for "a first transistor circuit that is arranged to deactivate the power device when a short-circuit detection signal is asserted". These structural requirements are simply not met by transistor 110 that instead just tracks the current in transistor 102 (See *D'Angelo* at col. 5, lines 13-18).

The Office Action states that "when the output is shorted, the voltage at the source of 110 will necessarily be pulled down...causing a high to be output from comparator 114. This, in turn, will cause transistor 102 to turn off." The Applicant respectfully disagrees that when the output is shorted, the source of 110 may be pulled down and amplifier 114. Instead, the **drain** of 110 is pulled down, but limited by the Vgs of 110 which is controlled by amplifier 114. Moreover, Pilot transistor 110 is not arranged to deactivate transistor 102. As the Office Action explains, it is the output **from the amplifier 114** that deactivates transistor 102, not the pilot transistor 110 (See *D'Angelo* at col. 6, rows 1-5). In contrast, Claim 1 describes "a first transistor circuit that is arranged to deactivate the power device."

In addition, transistors 120 do not meet the structural limitations of the second transistor circuit described in Applicant's Claim 1. Although transistors 120 can generically be referred to as a second transistor(s), the structural limitations of "a second transistor circuit" from Applicant's Claim 1 requires that the second transistor circuit be arranged in relation to the remaining claim elements. Applicant's Claim 1 does not call merely for a transistor, and instead calls for "a second transistor circuit ... **arranged to couple a small current to the load circuit** when the short-circuit detection signal is asserted **such that** the apparatus automatically **returns**

to a normal operating mode when the short-circuit condition is removed." These structural relationships are simply not met by transistors 120.

Instead, transistors 120 are taught as part of a current mirror circuit (See *D'Angelo* at col. 5, lines 27 - 30) that can be selectively disabled by transistors 140 - 146, which operate as bypass switches (See *D'Angelo* at col. 6, lines 40 - 48). Further, neither the drain nor the source of transistors 120 is coupled to the load (See *D'Angelo* at Figure 5). With neither the drain nor the source coupled to the load (See *D'Angelo* at Figure 5, node 122), transistors 120 cannot be arranged to couple a small current to the load circuit such that the apparatus automatically returns to a normal operating mode as is described in Applicant's Claim 1. Accordingly, *D'Angelo* fails to meet the structural limitations of Applicant's Claim 1. For at least these reasons, Claim 1 is submitted to be patentable and allowance is solicited.

Regarding Claims 5-8 and 12, dependant Claims 5-8 and 12 depend from and further limit Claim 1 and should be allowable for at least that reason as well as any additional limitations they recite.

Regarding Claim 13, Applicant's Claim 13 has been amended in a in a similar manner to amended Claim 1 and is submitted to be patentable for at least the reasons stated above.

Regarding Claims 14-16, dependant Claims 14-16 depend from and further limit amended Claim 13 and should be allowable for at least that reason as well as any additional limitations they recite.

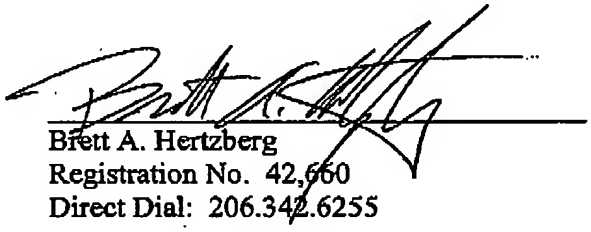
Regarding Claim 17, Applicant's Claim 17 has been amended in a in a similar manner to amended Claim 1 and is submitted to be patentable for at least the reasons stated above.

Regarding Claims 18-20, dependant Claims 18-20 depend from and further limit amended Claim 17 and should be allowable for at least that reason as well as any additional limitations they recite.

In view of the foregoing amendments and remarks, all pending claims are believed to be allowable and the application is in condition for allowance. Therefore, a Notice of Allowance is respectfully requested. Should the Examiner have any further issues regarding this application, the Examiner is requested to contact the undersigned attorney for the applicant at the telephone number provided below.

Respectfully submitted,

MERCHANT & GOULD P.C.



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